COMMON-MODE AND DIFFERENTIAL-MODE COMPENSATION FOR OPERATIONAL AMPLIFIER CIRCUITS

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Priority Claim

[0001] The present application claims priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application No. 60/413,896, entitled "Common-Mode and Differential-Mode Compensation for Operational Amplifier Circuits," which was filed on September 25, 2002.

Field of the Invention

[0002] The present invention relates to frequency compensation provided for operational amplifiers connected to provide two different signal paths, one for common-mode signals and another for differential mode signals.

Background

[0003] Operational amplifiers are prone to instability and, thus, require some means of frequency compensation to ensure reliable stable operation. Fig. 1 shows a commonly used compensation technique used in an operational amplifier 100. The amplifier 100 includes a transconductance stage 102, a compensation capacitor (C_{COMP}) 104 and high-impedance resistor (R_{HI}) 106 connected to the gain node n105, and a buffer 108 connecting the gain node to the amplifier output.

[0004] The compensation technique used in Fig. 1 includes placing the compensation capacitor 104 at the high-impedance gain node n105 to reduce the amplifier gain at high frequency, thus introduces a dominant pole into the open-loop frequency response of the operational amplifier 100. The dominant pole then occurs at a frequency f_p calculated as follows:

$$f_p = 1/(2\pi R_{HI} C_{COMP})$$

The minimum value of compensation capacitor (C_{COMP}) required to guarantee stable operation depends on many factors, including external feedback and the load impedance at the amplifier's output.

[0005] Often two of the operational amplifiers 100, as shown in Fig. 1, will be interconnected to form a differential driver circuit, which contains both a differential and a common-mode signal path.. An example of two such interconnected amplifiers 200 and 202 is shown in Fig. 2. In Fig. 2, a common mode signal is applied by voltage source (V_{CM}) 220 to the non-inverting inputs of amplifiers AMP_A 200 and AMP_B 202, while a differential mode signal is supplied by voltage sources 232 and 230. Any arbitrary voltage input to the circuit in Fig. 2 can be represented as a sum of common-mode and differential input voltages. Feedback resistors 204 and 206, each having a resistance value R_F, are connected between the output of amplifiers 200 and 202 and their inverting inputs. A gain resistor 208, having a resistance $2R_G$, is further connected between the inverting inputs. A load impedance having the resistance R_L is connected between the outputs OUT_A and OUT_B of the respective amplifiers AMP_A 200 and AMP_B 202.

[0006] To illustrate why the compensation scheme of Fig. 1 is not optimal for the circuit of Fig. 2, consider the effect of the two independent signal paths on stability. Common-mode signals will not cause any current to flow through the gain resistor 208 and load resistor 210, and therefore the common-mode and differential signal paths will have different voltage/current feedback levels and load impedances. The differential output voltage V_{OD} and the common-mode output voltage V_{OC} are given as follows:

$$V_{OD} = V_{DIFF} (1 + R_F/R_G)$$

$$V_{OC} = V_{CM}$$

Therefore the common-mode signal path has a gain of unity and its output is unloaded, while the differential signal path has a higher gain and sees a resistive load.

[0007] Because of these differences the two signal paths will have different minimum values of C_{COMP} required to ensure stable operation. To guarantee stable operation of the entire circuit, the larger of these two values must be used. If, for example, the common-mode signal path requires a higher value of C_{COMP}, then the differential signal path will be "over-compensated", thus lowering signal bandwidths and slew rates and limiting overall amplifier performance.

[0008] One circuit modification to partially avoid this problem would be to replace the gain resistor 208 of Fig. 2 with the resistors 300 and 302 of Fig. 3 which connect the inverting inputs of amplifiers 200 and 202 to ground. With such a circuit both differential and common-mode signals cause current to flow through R_G. Therefore both signal paths see the same feedback levels and have the same closed-loop gain, and will require roughly the same value of C_{COMP}. However, the load impedance is still different for the two signal paths and some over-compensation is unavoidable. Additionally, the connection to ground in the circuit of Fig. 3 has several undesirable properties. Common-mode offset and noise voltages will be fully amplified, and because the two amplifiers are now isolated their output voltages and currents will not necessarily track each other. These effects will compromise differential signal performance.

SUMMARY

[0009] In accordance with the present invention, a compensation scheme is provided for two interconnected amplifier circuits which allows independent frequency compensation of the common-mode and/or differential signal paths. This method can be used to stabilize differential circuits without compromising performance through over-compensation, and without any need to isolate the amplifiers from one another.

[0010] A circuit in accordance with an embodiment of the present invention includes two operational amplifier amplifiers AMP_A and AMP_B. The amplifiers making up AMP_A and AMP_B

can use any operational amplifier topology including voltage feedback and current feedback methods, and can be made from any transistor technology including, but not limited to, bipolar and MOSFET devices. The amplifiers AMP_A and AMP_B each include a transconductance stage and output buffer, similar to Fig. 1. Circuitry is further included in each of AMP_A and AMP_B to form an inverter, with the inverter having an input connected to the gain node at the output of the transconductance stage.

[0011] Common mode compensation is provided by connecting capacitors from the gain node at the input of an inverter in one of the amplifiers AMP_A or AMP_B to the output of the inverter in the other amplifier. For the bipolar current feedback amplifiers, two capacitors having a value $C_{COMMON}/2$ are connected together in each of AMP_A and AMP_B on one end to the output of current mirrors which are connected to effectively form the output of the inverter, and separately to separate inputs of the current mirrors in the opposing AMP_A or AMP_B. For the MOSFET differential amplifiers, common mode compensation capacitors having a value C_{COMMON} are connected from the inverting output of one differential amplifier to the non-inverting output of the other differential amplifier.

[0012] Differential mode compensation can be provided by connecting a capacitor with value C_{COMP} from the gain node to ground of each of the amplifiers AMP_A or AMP_B, similar to the compensation provided in amplifier 100 of Fig. 1. Alternatively, both differential mode and Miller effect compensation can be provided by connecting capacitors from the input to the output of components forming the inverter in each of the amplifiers AMP_A and AMP_B. For the MOSFET differential amplifiers, differential and Miller effect compensation is provided by connecting a capacitor having a value C_{COMP} between the inverting and non-inverting outputs in each amplifier. For bipolar current feedback amplifiers, a capacitance of $C_{COMP/2}$ is connected between the output of current mirrors forming the gain node, and each current mirror input. As a further alternative, differential and common mode compensation can be provided independently by connecting a capacitor with value C_{DIFF} between the outputs of the inverters of the amplifiers AMP_A and AMP_B.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The present invention will be described with respect to particular embodiments, and references will be made to the drawings in which:

[0014] Fig. 1 shows a commonly used compensation technique for an operational amplifier;

[0015] Fig. 2 shows two of the operational amplifiers of Fig. 1 interconnected to drive both a differential signal and a common mode signal;

[0016] Fig. 3 shows gain resistors which may be used to replace the gain resistor of Fig. 2;

[0017] Fig. 4 shows an operational amplifier using a compensation technique in accordance with an embodiment of the present invention;

[0018] Fig. 5 shows circuitry implementing the block diagram of Fig. 4 using bipolar current-feedback amplifiers, according to an embodiment of the present invention;

[0019] Fig. 6 shows modifications to the circuit of Fig. 5 to provide Miller effect compensation, according to an embodiment of the present invention;

[0020] Fig. 7 shows modifications to Fig. 5 to enable common-mode signals and differential mode signals to be independently compensated, according to an embodiment of the present invention;

[0021] Fig. 8 shows the two amplifiers of Fig. 4 created using MOSFET voltage-feedback differential amplifiers, according to an embodiment of the present invention;

[0022] Fig. 9 shows modifications to the circuit of Fig. 8 to provide differential mode compensation as in the circuits of Figs. 4 and 5, according to an embodiment of the present invention; and

[0023] Fig. 10 shows modifications to the circuit of Fig. 8 to provide differential mode compensation along with Miller effect compensation, according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0024] Fig. 4 shows an operational amplifier using a compensation technique in accordance with embodiments of the present invention. The circuit of Fig. 4 includes two amplifiers, AMP_A 400 and AMP_B 460. The amplifier AMP_A 400 includes a transconductance amplifier 401, high impedance node resistor 404, compensation capacitor 402, and output buffer 409, similar to the components of Fig. 1. Similarly, amplifier AMP_B 460 includes a transconductance amplifier 410, high impedance node resistor 414, compensation capacitor 412, and output buffer 419, as in Fig. 1.

[0025] Unlike the components of Fig. 1, the amplifier AMP_A 400 further includes an inverter 406 and common mode compensation capacitor C_{COMMON} 408 connected in series. The input of the inverter 406 is connected to the gain node n405 of the amplifier AMP_A 400, and the output of the capacitor C_{COMMON} 408 is connected to the gain node n415 of the amplifier AMP_B 460. Similarly, the amplifier AMP_B 460 includes an inverter 416 and common mode compensation capacitor C_{COMMON} 418 connected in series. The input of the inverter 416 is connected to the gain node n415 of the amplifier AMP_B 460, and the output of the capacitor C_{COMMON} 418 is connected to the gain node n405 of the amplifier AMP_A 400.

[0026] In operation, it is first assumed that a differential input signal is applied, so any signal at the input of amplifier AMP_A 400 is the opposite in sign to the input signal of amplifier AMP_B 460. V_A is defined as the voltage at the gain node n405, V_B is the voltage at gain node n415, V'_A is the voltage at the output of inverter 406, and V'_B being the voltage at the output of inverter. The following relations then exist:

$$V_A = -V_B$$
$$V'_A = -V_A = V_B$$
$$V'_B = -V_B = V_A$$

$$V'_A - V_B = V'_B - V_A = 0$$

Therefore in the case of the differential input signal, the voltages across the capacitors C_{COMMON} 408 and C_{COMMON} 418 are equal to zero. These two capacitors thus have no effect on differential signals, and the effective differential compensation capacitance is equal to C_{COMP}, as was the case in Fig. 1:

$$C_{EFF,\,DIFF} = C_{COMP}$$

[0027] In contrast, for the case of a common-mode signal, it is assumed that any signal at the input of amplifier AMP_A 400 is equal to the input signal of amplifier AMP_B 460. Using the voltage definitions from the previous passage, the relevant relations are now as follows:

$$V_A = V_B$$
$$V'_A = -V_A = -V_B$$
$$V'_B = -V_B = V_A$$

$$V'_A - V_B = V'_B - V_A = 2V_A = 2V_B$$

With these relations, the voltage across the capacitor C_{COMMON} 408 (V'_A-$V_B = 2V_A$) will be twice the voltage difference across the capacitor C_{COMP} 404 (V_A). Similarly, the voltage across the capacitor C_{COMMON} 418 ($V'_B - V_A = 2V_B$) will be twice the voltage difference across the capacitor C_{COMP} (V_B). Thus, the total effective common-mode compensation capacitance provided at either node n405 or n415, $C_{EFF,CM}$, is:

$$C_{EFF,CM} = C_{COMP} + 2C_{COMMON}$$

Therefore, with C_{COMP} compensating for differential mode and C_{COMMON} compensating for the common mode, the common mode and the differential mode are both compensated, and common mode instabilities can be mitigated without compromising differential mode performance.

[0028] Implementation of the block diagram of Fig. 4 using bipolar current-feedback amplifiers is shown in Fig. 5. As in Fig. 4, the operational amplifier of Fig. 5 includes an AMP_A 400 and an AMP_B 460. For convenience, components carried over from Fig. 4 to Fig. 5 are similarly labeled, as will be components carried over in subsequent drawings.

[0029] The current feedback amplifier of AMP_A 400 includes an NPN transistor 501 and a PNP transistor 502 having common bases forming the non-inverting input of the amplifier AMP_A 400. The transistor 501 has a collector connected to a power supply rail Vcc, and an emitter connected by a current sink 506 to a power supply rail Vee. The transistor 501 has its emitter connected through a current sink 508 to the power supply rail Vcc, and its collector connected to the power supply rail Vee. The emitter of transistor 502 is further connected to the base of NPN transistor 503, while the emitter of transistor 501 is connected to the base of PNP transistor 504. Transistors 503 and 504 are connected in an emitter follower configuration with the collector of transistor 503 connected to an input terminal of current mirror 510, and the collector of transistor 504 connected to an input terminal of current mirror 512. The outputs of the current mirrors 510 and 512 are connected to form the gain node n405. The gain node n405 is connected through buffer 409 to form the output OUT_A of the amplifier AMP_A 400.

[0030] The current mirror 510 includes PNP transistors 521 and 522 having common bases, and emitters connected to the voltage supply rail Vcc. The collector of transistor 521 forms the current mirror input connected to transistor 503. The collector of transistor 522 is connected to its base, as well as to the emitter of transistor 523. Transistor 523 has a base connected to the collector of transistor 521 and a collector forming an output of the current mirror 510. The current mirror 512 includes transistors 531 and 532 connected in a common base configuration, similar to transistors 521 and 522 of current mirror 510. Transistor 533 in current mirror 512 is connected similar to transistor 523. The outputs of the current mirrors 510 and 512 at the collectors of transistors 523 and 533, effectively form the inverter 406 of Fig. 4. The transistors 523 and 533 function to reduce the effect of variations of the voltage rails Vcc and Vee. Although a particular configuration is shown for current mirrors 510 and 512, other configurations could be used, such as by removing transistors 523 and 533 and connecting the collectors of transistors 522 and 532 directly to the gain node.

[0031] To provide for differential mode compensation, capacitor C_{COMP} 402 is connected to the gain node n405. The collectors of transistors 523 and 533 provide a high impedance,

eliminating the need for the resistors R_{HI} 404 and 414 of Fig. 4. To provide for common mode compensation, capacitors 514 and 516 with a value $C_{COMMON}/2$ are connected together on one end, and to the collector of the respective transistors 503 and 504 at the other end.

[0032] The current feedback amplifier further includes AMP_B 460 made up of NPN transistor 551 and PNP transistor 552 having common bases forming the non-inverting input of the amplifier AMP_B 460, similar to transistors 501 and 502 of AMP_A 400. The transistors 551 and 552 are connected by respective current sinks 556 and 558 to the power supply rails Vcc and Vee. The amplifier AMP_B 460 further includes emitter follower transistors 553 and 554 connected to current mirrors 560 and 562, similar to the emitter follower transistors 503 and 504 connected to current mirrors 510 and 512 of AMP_A 400. The outputs of the current mirrors 560 and 562 form the gain node n415 for AMP_B 460. The current mirrors 560 and 562 have components similar to current mirrors 510 and 512 of AMP_A 400. The gain node n415 is connected by a buffer 419 to form the amplifier output OUT_B.

[0033] To provide compensation, a differential mode capacitor 412 having a value C_{COMP} is connected from the gain node n415 to ground. Common mode compensation capacitors 564 and 566 with values $C_{COMMON/2}$ have first ends connected to the collectors of respective transistors 553 and 554, and second ends connected together to the gain node n405 of AMP_A 400. The connected terminals of the common mode compensation capacitors 514 and 516 of AMP_A 400 are likewise connected to the gain node n415 of AMP_B 460.

[0034] In the circuit of Fig. 5 the current mirrors are playing a dual role, being both part of the transconductance stage and also providing voltage inversion. For example, in current mirror 510 voltage inversion is obtained between the collectors of transistors 521 and 523. This voltage inversion plays the role of voltage inverters 406 and 416 in Fig. 4, and the effective differential and common-mode compensation can be calculated as above. Similar comments apply to the current mirrors in the remaining figures.

[0035] Fig. 6 shows modifications to the circuit of Fig. 5 to provide Miller effect compensation. Fig. 6 removes the differential mode compensation capacitors 402 and 412,

having a value C_{COMP}, from Fig. 5. Capacitor 402 is replaced with capacitors 601 and 602, each having a value $C_{COMP/2}$. Capacitor 412 is replaced with capacitors 604 and 606, each having the value $C_{COMP/2}$. Capacitors 601 and 602 are connected on a first terminal to the gain node n405, and on a second terminal to the collector of respective transistors 503 and 504. Capacitors 604 and 606 are connected on a first terminal to the gain node n415, and on a second terminal to the collector of respective transistors 553 and 554. Apart from providing Miller effect compensation, the circuit of Fig. 6 functions in a substantially similar manner to the circuit of Fig. 5.

[0036] Fig. 7 shows modifications to Fig. 5 to enable common-mode signals and differential mode signals to be independently compensated. In Fig. 7, the compensation capacitors 402 and 412, having a value C_{COMP}, from Fig. 5 are replaced by a single compensation capacitor 709 having a value C_{DIFF}. The capacitor 709 is connected between the gain nodes n405 and n415 of the amplifiers AMP_A 400 and AMP_B 460. In operation with only common mode signals, the capacitor 709 with value C_{DIFF} would see no voltage difference across its terminals, but for only differential mode signals, the capacitor 709 would see twice the differential voltage across its terminals. Similarly, the common mode capacitors 514, 516, 564 and 566, each with a value $C_{COMMON/2}$, would see no voltage difference across their terminals for differential mode signals, but would see twice the common mode voltage. Accordingly, the equivalent common mode and differential mode capacitance compensation values can be independently specified as follows:

$$C_{COMP\text{-}DM} = 2\, C_{DIFF}$$
$$C_{COMP\text{-}CM} = 2\, C_{COMMON}$$

[0037] Fig. 8 shows amplifiers AMP_A 400 and AMP_B 460 of Fig. 4 created using MOSFET voltage-feedback differential amplifiers. The amplifier AMP_A 400 includes differentially connected NMOS transistors 801 and 802, each with a gate forming a respective input of the amplifier 400, and sources connected together through a current sink 806 to V_{SS}. A

current mirror 804 has terminals connected to the respective drains of the transistors 801 and 802. The drain of transistor 802 is also connected through buffer 409 to form the output OUT_A. The drain of transistor 801 is further connected to a first terminal of the common mode compensation capacitor 408 having a value C_{COMMON}.

[0038] Similar to the AMP_A 400, the amplifier AMP_B 460 includes differentially connected NMOS transistors 821 and 822, each with a gate forming a respective input of the amplifier AMP_B 460, and sources connected together through a current sink 826 to V_{SS}. A current mirror 824 has terminals connected to the respective drains of the transistors 821 and 824. The drain of transistor 821 is connected through buffer 419 to form the output OUT_B. The drain of 821 is connected to a first terminal of a common mode compensation capacitor 418 having a value C_{COMMON}.

[0039] The current mirror 804 of AMP_A 400 includes two PMOS transistors 810 and 811 connected with common gates, and sources connected to the power supply rail V_{DD}. A second set of PMOS transistors 814 and 815 are also connected with common gates. The drains of transistors 814 and 815 form the input and output terminals of the current mirror 804. The drain and gate of transistor 810 is connected to the source of transistor 814. The drain of transistor 811 is connected to the source of transistor 815. The gate of transistor 814 is connected to its drain.

[0040] The current mirror 824 of AMP_B 460 includes transistors 830, 831, 834 and 835 connected in a manner similar to the connection of transistors 810, 811, 814 and 815 of AMP_A 400. The transistors 814, 815, 834 and 835 serve to isolate the outputs OUT_A and OUT_B from variations in the power supply voltage V_{DD}. Although one configuration of transistors forming a current mirror is shown for current mirrors 804 and 824, other configurations might be used, such as eliminating transistors 814, 815, 834 and 835 and using the drains of transistors 810, 811, 830 and 831 as terminals of the current mirrors 804 and 824.

[0041] A compensation scheme similar to Fig. 7, with independent common mode and differential mode compensation is used in Fig. 8. As in Fig. 7, a differential mode compensation capacitor 709 having a value C_{DIFF} is connected between the gain nodes n405 and n415 of the

amplifiers AMP_A 400 and AMP_B 460. A second terminal of the common mode compensation capacitors 418 and 408, each having a value C_{COMMON}, is connected to a respective gain node terminals n405 and n415.

[0042] Although Fig. 8 shows one configuration for providing compensation for both differential and common mode signals, other configurations are available in accordance with the present invention. Figs. 9 and 10 show alternative configurations to Fig. 8 for providing differential mode compensation with amplifiers AMP_A 400 and AMP_B 460 still using MOSFET differential amplifiers.

[0043] Fig. 9 shows modifications to the circuit of Fig. 8 to provide single-ended compensation, as in the circuits of Figs. 4 and 5. The differential mode capacitor 709 of Fig. 8 having a capacitance value C_{DIFF} is removed, and differential mode compensation capacitors 402 and 412, each having a value C_{COMP} are used. Capacitor 402 is connected from the gain node n405 to V_{SS}, while the capacitor 412 is connected from the gain node n415 to V_{SS}.

[0044] Fig. 10 shows modifications to the circuit of Fig. 8 to provide differential mode compensation similar to the circuit of Fig. 6. In Fig. 10, the differential mode capacitor 709 from Fig. 8 is removed and differential mode capacitors 1002 and 1004, each having a value C_{COMP} are used. Capacitor 1002 is connected from node n405 to the drain of transistor 801, while the capacitor 1004 is connected from the gain node n415 to the drain of transistor 821. The capacitors 1002 and 1004 differ from the configuration of Fig. 9 in that Miller effect compensation is provided. Although the configurations of Fig. 9 and Fig. 10 offer alternatives to Fig. 8, they do not provide independent common mode and differential mode compensation, since the capacitors having a value C_{COMP} used in Figs. 9 and 10 provide some common mode compensation, as well as differential mode compensation.

[0045] Although the present invention has been described above with particularity, this was merely to teach one of ordinary skill in the art how to make and use the invention. Many other modifications will fall within the scope of the invention, as that scope is defined by the claims provided to follow.